Amendments to the Claims:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-3. (Canceled)

4. (Previously Presented) An erasable and programmable non-volatile cell, comprising:

an n-channel transistor having a source, a drain and a gate;

a floating capacitor having a floating gate and a control gate, said floating gate being connected to said gate of said n-channel transistor; and

circuitry for detecting the state, whether erased or programmed, of the cell,

wherein said circuitry for detecting the state of the cell comprises a p-channel transistor having a source, a drain and a gate, said p-channel transistor being complementary to said n-channel transistor and said gate of said p-channel transistor being connected to said floating gate

wherein an n-well diffusion region of said p-channel transistor is the control gate of said floating capacitor.

5-8. (Canceled)

9. (Currently Amended) The cell of claim [[1]]4, wherein the floating gate and the gates of the first and second transistors are embodied as a single polymer layer.

10. (Currently Amended) ~~An erasable and programmable non-volatile cell, comprising:~~

~~an n-channel transistor having a gate, a source, and a drain;~~

~~a p-channel transistor having a gate, a source, and a drain;~~

~~a floating capacitor having a floating gate and a control gate, wherein the floating gate is connected to the gate of the n-channel transistor;~~ The cell of claim 4,

wherein the n-channel transistor is adapted to program a data value into the cell by having appropriate programming voltages applied to its gate, source and drain, and

wherein the p-channel transistor is adapted to read the data value from the cell by having appropriate read voltages applied to its gate, source and drain.

11. (Currently Amended) The cell of claim [[11]]10, wherein the drain of the p-channel transistor is adapted to float when the data value is programmed into the cell, and wherein the drain of the n-channel transistor is adapted to float when the data value is read from the cell.

12-13. (Canceled)